CLAIM:

1. A processor (106) on an integrated circuit (102), the processor having a two-dimensional array of processing cells (108) and a mechanism (110) for reconfigurably connecting a plurality of paths to the array to respective cells (112) on a periphery of the array, the processor performing mathematical operations whose timing is based on a flow of input operands along the paths (218, 220).

The processor of claim 1, wherein the array comprises a systolic processing array (108).

3. The processor of claim 1, wherein the integrated circuit further comprises an analog circuit (304) in communicative connection with said processor.

4. A receiver (100) comprising the integrated circuit of claim 3.

5. The processor of claim 1, wherein inter-cell connection within the array is such that each cell of the array is connected only to cells whose column is the same and whose row is immediately adjacent, and only to cells whose row is the same and whose column is immediately adjacent (112).

6. The processor of claim 1, further comprising an input/output pad (118) of the processor along each of the plural paths.

7. The processor of claim 1, further comprising one or more input/output pads (118) of the processor along respective ones of the paths, wherein the integrated circuit includes in communicative connection with said processor an analog circuit (304), a digital circuit (302) and an analog-to-digital converter (314) connected to the digital circuit by a reconfigurable switch (110) configured to switch between a signal pathway from the analog circuit to the digital circuit and a signal pathway to or from said one or more input/output pads (118).

8. The processor of claim 1, wherein each path traverses a border cell (114) connected to a corresponding one of said respective cells (112) so that the reconfiguring of a path causes the path to traverse at least one of a different border cell and a different I/O pad (118, 122, 124).

9. The processor of claim 1, wherein the mechanism comprises a crossbar network (120).

10. The processor of claim 1, wherein the paths are connected one-to-one with said respective cells (122, 124).

11. The processor of claim 10, wherein said input operands are buffered on their respective paths before arrival at the array (214), said performing not commencing before a corresponding predetermined number of operands is buffered for each respective path of a predefined subset of the paths (230), said number being one or greater.

12. The processor of claim 10, wherein said input operands are buffered on their respective paths before arrival at the array (214), said performing not commencing before a corresponding predetermined number of operands that have been buffered for each respective path of a predefined subset of the paths have been found to be valid (230), said number being greater than one.

13. The processor of claim 12, further including a bus to which the array cells (112) are connected and by means of which the array cells are programmable (202).

14. The processor of claim 13, further comprising on the bus a master cell (126) for reprogramming the array cells (202).

15. The processor of claim 14, wherein said master cell (126) commences said performing (230).

16. The processor of claim 1, further including a bus to which the array cells (112) are connected and by means of which the array cells are programmable (202).

17. The processor of claim 1, including an array processor that comprises said two-dimensional array (108).

18. The processor of claim 1, wherein said array is rectangular and said periphery consists of those of said processing cells (112) located in at least one of a first row, last row, first column and last column of said array.

19. The processor of claim 1, wherein the paths include first-in/first-out (FIFO) buffers that are configured in a Kahn process network implemented to stall a process from writing to a buffer of said buffers if the buffer is full (228).

20. A method comprising the steps of:

providing on an integrated circuit (102) a processor (106) having a two-dimensional array of processing cells (108) and a mechanism (110) for reconfigurably connecting a plurality of paths to the array to respective cells (112) on a periphery of the array; and

utilizing the processor to perform mathematical operations whose timing is based on a flow of input operands along the paths (218, 220).